In Claims:

Cancel claims 23, 25, 31 and 32 without prejudice.

Rewrite the pending claims and add new claims to read as follows:

1. (Currently Amended) A semiconductor package, comprising:

a chip carrier to receive a semiconductor with a dimension greater than 26 mm, said chip carrier having a first coefficient of thermal expansion different than the coefficient of thermal expansion of said semiconductor; and

a stress inhibiting intermediate mounting substrate connected to said chip carrier through a first array of solder connections, said stress inhibiting intermediate mounting substrate being adapted for connection to ~~an interposer~~ a printed circuit board through a second array of solder connections, said stress inhibiting intermediate mounting substrate having a second coefficient of thermal expansion different than the coefficient of thermal expansion of said chip carrier and smaller than the coefficient of thermal expansion of said ~~interposer~~ printed circuit board, and said stress inhibiting intermediate mounting substrate being adapted for allowing access through the substrate to one or more solder connections in the first array.

2. (Currently Amended) The semiconductor package of claim 1 wherein said ~~interposer~~ stress inhibiting intermediate mounting substrate is a printed circuit board.

3. (Original) The semiconductor package of claim 1 wherein said chip carrier is formed of a ceramic material.

4. (Original) The semiconductor package of claim 3 wherein said chip carrier has a CTE between 3 and 7 PPM.

5. (Original) The semiconductor package of claim 1 wherein the first coefficient of thermal expansion is larger than the coefficient of thermal expansion of said semiconductor.

6. (Original) The semiconductor package of claim 1 wherein the second coefficient of thermal expansion is larger than the coefficient of thermal expansion of said chip carrier.

7. (Original) The semiconductor package of claim 5 wherein the second coefficient of thermal expansion is larger than the coefficient of thermal expansion of said chip carrier.

8. (Original) The semiconductor package of claim 6 wherein the second coefficient of thermal expansion is smaller than the coefficient of thermal expansion of said printed circuit board.

9. (Original) The semiconductor package of claim 1 wherein the second coefficient of thermal expansion is between 14 and 18 PPM.

10. (Original) The semiconductor package of claim 1 further comprising solder bumps positioned on said chip carrier to facilitate connection with said semiconductor.

11. (Original) The semiconductor package of claim 10 wherein the solder bumps are lead-free.

12. (Original) The semiconductor package of claim 1 wherein at least one solder connection is lead-free.

13. (Original) The semiconductor package of claim 1 further comprising a semiconductor having a dimension greater than 26 mm mounted to the chip carrier.

14. (Currently Amended) The semiconductor package of claim 1 further comprising under-fill resin positioned between said ~~solder bumps~~ first array of solder connections.

15. (Original) The semiconductor package of claim 1 further comprising a lid positioned over said chip carrier.

16. (Original) The semiconductor package of claim 1 wherein said stress inhibiting mounting substrate includes signal paths between a top surface of said stress inhibiting mounting substrate and a bottom surface of said stress inhibiting mounting substrate.

17. (Currently Amended) A semiconductor package comprising:

a chip carrier to receive a semiconductor said semiconductor having a dimension greater than 26 mm and said chip carrier having a first coefficient of thermal expansion between 3 and 7 PPM; and

a stress inhibiting mounting substrate connected to said chip carrier through a first array of solder connections, said stress inhibiting intermediate mounting substrate being adapted for allowing access through the substrate to one or more solder connections in the first array.

18. (Original) The semiconductor package of claim 17 wherein said stress inhibiting mounting substrate has a coefficient of thermal expansion between 14 and 18 PPM.

19. (Original) The semiconductor package of claim 17 further comprising a printed circuit board mounting substrate connected to said stress inhibiting mounting substrate through a second array of solder connections, said printed circuit board mounting substrate having a coefficient of thermal expansion between 14 and 17 PPM.

20. (Original) The semiconductor package of claim 18 further comprising a printed circuit board mounting substrate connected to said chip carrier through a second array of solder connections, said printed circuit board mounting substrate having a coefficient of thermal expansion between 14 and 17 PPM.

21. (Currently Amended) The semiconductor package of claim 17 further comprising ~~further comprising~~ a semiconductor having a dimension greater than 26 mm mounted to the chip carrier.

22. (Currently Amended) A semiconductor package, comprising:

a chip carrier to ~~receive~~ which a semiconductor is connected by an array of solder bumps;

a stress inhibiting intermediate mounting substrate connected to said chip carrier through a first array of solder connections, said substrate being adapted for allowing access through the substrate to one or more solder connections.

23. (Canceled) The semiconductor package of claim 22 further comprising further comprising a semiconductor mounted to the chip carrier.

24. (Currently Amended) The semiconductor package of claim 22 further ~~comprises~~ comprising ~~an interposer~~ a printed circuit board connected to said substrate through a second array of solder connections, said ~~interposer~~ printed circuit board being adapted for allowing access through the substrate to one or more solder connections of the first array of solder connections.

25. (Canceled) The semiconductor package of claim 24 wherein said interposer is a printed circuit board.

26. (Original) The semiconductor package of claim 22 wherein said access permits the removal of flux.

27. (Original) The semiconductor package of claim 22 wherein said access permits the cleaning of flux.

28. (Currently Amended) The semiconductor package of claim 22 wherein said access permits the insertion of ~~under-fill~~ underfill material.

29. (Currently Amended) The semiconductor package of claim 22 wherein the substrate further includes ~~at least one additional row~~ a plurality of rows of solder connections ~~adjacent to a row of solder connections of the array of solder connections~~ wherein the number of solder connections in ~~the~~ at least one ~~additional~~ row is less than the number of solder connections in each row of solder connections of a subset of the ~~array~~ plurality of solder connections because of the absence of solder connections at or near one or more corners of the substrate

30. (Currently Amended) A substrate having a through-hole channel located at or near a center of the substrate and a ~~first row~~ plurality of rows of solder connections ~~adjacent to a row of solder connections of an array of solder connections~~ wherein the number of solder connections in a first row is less than the number of solder connections in each row of solder connections of a subset of the ~~array~~ plurality of solder connections because of the absence of solder connections at or near one or more corners of the substrate.

31. (Canceled) A method of underfilling a gap between a multi-sided semiconductor device and a substrate to encapsulate a plurality of electrical connections formed therebetween, comprising:

forming a channel between said device and said substrate;

leaving said channel open to at least one side of said device to permit access to said device; and

dispensing an under-fill material adjacent said at least one side of said device through said channel.

32. (Canceled) The method of claim 31 wherein said channel permits the removal of residual flux.

33. (New) The semiconductor package of claim 22 wherein the chip carrier includes a passage allowing access through the chip carrier to one or more solder connections.

REMARKS

This is to affirm the election of group I, claims 1-30 made on February 28, 2003, for prosecution in this application.

In the Office Action mailed April 16, 2003:

- Claims 21, 22, 24 and 28 were objected to because of certain minor informalities which have been corrected in this amendment.
- Claims 1-16, 24-25, 29 and 30 were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.
- Claims 1-16 and 24-25 were also rejected under 35 U.S.C. 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- Claims 1-10, 13, 14 and 16 (as best understood by the Examiner in view of the 35 U.S.C. § 112, 2nd paragraph rejection above) and 17-21 were rejected under 35 U.S.C. 103(a) as unpatentable over Alagaratnam et al. (USP 6,335,491).
- Claims 11 and 12 (as best understood by the Examiner in view of the 35 U.S.C. § 112, 2nd paragraph rejections, above) were rejected under 35 U.S.C. 103(a) as unpatentable over Alagaratnam et al. in view of Jackson et al. (USP 6,333,563).
- Claim 15 (as best understood by the Examiner in view of the 35 U.S.C. § 112, 2nd paragraph rejections, above) was rejected under 35 U.S.C. 103(a) as unpatentable over Alagaratnam et al. in view of Suzuki (USP 5,650,918).
- Claims 22, 23 and 28 were rejected under 35 U.S.C. 102(b) as anticipated by Moore et al. (USP 5,120,678).
- Claims 26 and 27 were rejected under 35 U.S.C. 103(a) as unpatentable over Moore et al. in view of Degani et al. (USP 6,074,897).
- Claim 29 was rejected under 35 U.S.C. 103(a) as unpatentable over Moore et al. in view of Lyne (USP 6,285,560).
- Claim 30 was rejected under 35 U.S.C. 102(b) as anticipated by Beilin et al. (USP 5,854,534) or by Kikuchi et al. (USP 5,849,606).

In addition, the drawings were objected to for failing to disclose an element claimed in claims 29 and 30.

With this amendment, claims 1-2, 14, 17, 21-22, 24 and 28-30 have been amended to address the rejections and objections raised by the Examiner in the Office Action. Claim 33 is a new claim. No new matter has been entered. Reconsideration of the rejection against claims 1-30 is respectfully requested.

Drawing Objection

Claim 29 has been amended to recite that the number of solder connections in at least one row is less than the number of solder connections in each row of solder connections of a subset of the rows of solder connections and that this is achieved by the absence of solder connections at or near one or more corners of the substrate. Claim 30 has been amended to recite that there is a through-hole channel located at or near the center of the substrate, that the number of solder connections in a first row is less than the number of solder connections in each row of solder connections of a subset of the rows of solder connections and that the reduced number of solder connections is achieved by the absence of solder connections at or near one or more corners of the substrate.

As shown in Fig. 6, there is a through-hole channel 650 at the center region of substrate 600 and the array of solder connections has a total of 16 rows. Among them, each of the top row, the bottom row and the two rows in the middle of the array has 16 solder connections, while each of the other 12 rows has 18 solder connections. In other words, the number of solder connections of at least one row, i.e., both the top and bottom rows, is less than the number of solder connections in each row of a subset of the array, i.e., the 12 rows that have 18 solder connections. Fig. 6 also illustrates the reduced number of solder connections in the top and bottom rows , resulting from the absence of solder connections at the four corners 610, 620, 630, and 640 of substrate 600. *See* page 9, lines 19-24.

Since all the features in claims 29 and 30 have been shown in Fig. 6 and described in the specification, the objection to Fig. 6 has been obviated.

Claim Objections

The second occurrence of "further comprising" in claim 21 has been deleted, "allow" in claims 22 and 24 has been replaced with "allowing", claim 23 has been canceled, "comprises" in claim 24 has been replaced with "comprising", and "under-fill" in claim 28

has been replaced with "underfill". Therefore, the objections to claims 21-24 and 28 have been obviated.

Claim Rejections - 35 U.S.C. 112, first paragraph

The Examiner has correctly pointed out that the term "interposer" in claims 1 and 24 should be "printed circuit board". *See* page 5, lines 11-15. In this response, claims 1 and 24 have been amended by replacing "interposer" with "printed circuit board". Claim 2 has been amended as suggested by the Examiner to describe the stress inhibiting intermediate mounting substrate as a printed circuit board. This amendment is supported by page 8, lines 15-16 of the specification. The amendments to claims 29 and 30 have been discussed above. Claims 3-16 are dependent upon claims 1 and 24, respectively. Therefore, the rejections to claims 1-16, 24, 29 and 30 under 35 U.S.C 112, first paragraph, should be withdrawn.

Claim Rejections - 35 U.S.C. 112, second paragraph

The amendment to claim 1 to replace "interposer" with "printed circuit board" has been discussed above. This provides the antecedent for the limitation "said printed circuit board" in claim 8. Claim 2 has been amended by replacing "said interposer" with "said stress inhibiting intermediate mounting substrate". *See* page 9, lines 6-7. Claim 14 has been amended by replacing "solder bumps" with "first array of solder connections" first appearing in claim 1. *See* page 6, lines 17-18. The amendment to claim 24 has been discussed above. Claims 2-16 are dependent upon claim 1. Therefore, the rejections to claims 1-16 under 35 U.S.C. 112, second paragraph, should be withdrawn

Claim Rejections - 35 U.S.C. 102

Claim 22 has been amended to recite that a semiconductor is connected to a chip carrier by an array of solder bumps and that a stress inhibiting intermediate mounting substrate is connected to the chip carrier through a first array of solder connections.

In contrast, Moore et al. only describes an electronic component 92 comprising a semiconductor chip 100 mounted on an alumina carrier 102 and connected to through-conductors 104 by wire leads 105. Moore et al. does not disclose that semiconductor chip 100 is mounted on an alumina carrier 102 by an array of solder bumps as claim 22 recites. In addition, Moore et al. does not teach that a stress inhibiting intermediate mounting substrate

is connected to the chip carrier through a first array of solder connections. Substrate 106 of Moore et al. is not a stress inhibiting intermediate mounting substrate as recited in claim 22, but is an epoxy-glass laminate base that is part of the printed circuit board 94. *See* Figs. 2-5 and column 6, lines 30-32 of Moore et al. Therefore, claim 22 and dependent claim 28 are not anticipated by Moore et al.

Claim 30 has been amended by inserting limitations "a through-hole channel located at or near a center of the substrate", "of a subset" and "the absence of solder connections at or near one or more corners of the substrate" into the claim. *See* Fig. 6 and page 9, lines 19-24.

Beilin et al. only discloses secondary substrates 602B at the four corners of a substrate 602 having a triangular array of wire interconnectors 608B. Beilin et al. does not disclose a through-hole channel located at or near the center of substrate 602 or any solder connection missing at any corner of substrate 602. As illustrated in Fig. 17A of Beilin et al., there is actually no through-hole channel at or near the center of substrate 602 and there is a wire interconnector 608B at every corner of substrate 602.

Similar to Beilin et al., while Kikuchi et al. discloses a semiconductor device 46 having connecting terminals 32 missing from one corner 35C of the device in Fig. 14(a), it does not disclose a through-hole channel located at or near the center of substrate 21.

Since neither Beilin et al. nor Kikuchi et al has disclosed all the limitations recited by claim 30, claim 30 is not anticipated by either of them.

Claim Rejections - 35 U.S.C. 103

To reject claims in an application under 35 U.S.C. 103, the Examiner bears the initial burden of establishing a prima facie case of obviousness. *In re Bell*, 26 USPQ2d 1529, 1530 (Fed. Cir. 1993). To establish prima facie obviousness, three basic criteria must be met. First, the prior art must provide one of ordinary skill in the art with a suggestion or motivation to modify or combine the teachings of the references relied upon by the PTO to arrive at the claimed invention. *WMS Gaming Inc. v. International Game Technology*, 51 USPQ2d 1385, 1397 (Fed. Cir. 1999). Second, the prior art must provide one of ordinary skill in the art with a reasonable expectation of success. *In re O'Farrell*, 7 USPQ2d 1673 (Fed. Cir. 1988); *In re Dow Chemical Co.*, 5 USPQ2d 1529, 1531 (Fed. Cir. 1988). Third, the prior art, either alone or in combination, must teach or suggest each and every limitation of the rejected claims. *In re Vaeck*, 20 USPQ2d 1438 (Fed. Cir. 1991); *In re Royka and*

Martin, 180 USPQ 580 (C.C.P.A. 1974); and *In re Wilson*, 165 USPQ 494 (C.C.P.A. 1970). The teaching or suggestion to make the claimed invention, as well as the reasonable expectation of success, must come from the prior art, not Applicant's disclosure. *In re Vaeck*, Id. If any one of these criteria is not met, prima facie obviousness is not established.

As discussed in detail below, the cited art fails to satisfy at least one of the three criteria. Therefore, the Applicant respectfully requests withdrawal of the rejections.

Claim 1 recites a semiconductor package comprising a chip carrier to receive a semiconductor with a dimension greater than 26 mm and a stress inhibiting intermediate mounting substrate connected to the chip carrier through a first array of solder connections. The substrate is adapted for connection to a printed circuit board through a second array of solder connections. The substrate is further adapted for allowing access through the substrate to one or more solder connections in the first array.

Similarly, claim 17 recites a semiconductor package comprising a chip carrier to receive a semiconductor having a dimension greater than 26 mm, said chip carrier having a first coefficient of thermal expansion between 3 and 7 PPM, and a stress inhibiting mounting substrate connected to said chip carrier through a first array of solder connections. The stress inhibiting intermediate mounting substrate is adapted for allowing access through the substrate to one or more solder connections in the first array.

In contrast, Alagaratnam et al. only discloses a semiconductor device 225 comprising an interposer 202 connected to a substrate 204 through a first array of solder balls 212 and a PCB 226 through a second array of solder balls 214. *See* Fig. 3 of Alagaratnam et al. However, Alagaratnam et al. does not teach that the interposer 202 is adapted for allowing access through the interposer to any solder ball in the first array. In addition, Alagaratnam et al. does not disclose an interposer suitable for a semiconductor with a dimension greater than 26 mm, since the interposer 202 is only suitable for a die size in the range of 10 mm to 20 mm. *See* column 6, lines 41-42, of Alagaratnam et al.

Since Alagaratnam et al. does not teach or suggest each and every limitation recited in claims 1 and 17, claims 1 and 17 are patentable over Alagaratnam et al.

Claims 2-16 and 18-21 are ultimately dependent upon claims 1 and 17 respectively. Therefore, claims 2-16 and 18-21 are patentable over Alagaratnam et al. for at least the same reason claims 1 and 17 are patentable.

In addition, claims 9 and 18 recite that the coefficient of thermal expansion of the stress inhibiting intermediate mounting substrate is between 14 and 18 PPM. In contrast, Alagaratnam et al. teaches at column 5, lines 55-57, that the CTE of the interposer 202 is approximately 12 PPM, not in the range recited in claims 9 and 18.

With respect to claims 26 and 27, Moore et al. does not disclose all the limitations of claim 22 on which these two claims depend. First, Moore et al. does not disclose a chip carrier to which a semiconductor is connected by an array of solder bumps. Second, Moore et al. does not disclose a stress inhibiting intermediate mounting substrate connected to the chip carrier through a first array of solder connections.

While Degani et al. discloses a substrate 10 having an aperture 30 for cleaning residual flux, Degani et al. does not disclose a chip carrier to which the IC chip 1 is connected, because the IC chip 1 is directly connected to the substrate 10. Even if the substrate 10 is treated as the chip carrier 102 in Moore et al., the combination of Moore et al. and Degani et al. still does not disclose the stress inhibiting intermediate mounting substrate adapted for allowing access through the substrate to one or more solder connections recited by claim 22, because substrate 106 in Moore et al. is part of PCB 94 and is not a stress inhibiting intermediate mounting substrate.

As shown in Fig. 5 of the present invention, the stress inhibiting intermediate mounting substrate 540 and the printed circuit board 550 are two separate components of a semiconductor package and the printed circuit board 550 does not have a through-hole channel. Since Moore et al. and Degani et al., either alone or jointly, do not teach every limitation of claims 26 and 27, claims 26 and 27 are patentable over Moore et al. in view of Degani et al.

Claim 29 recites a substrate connected to a chip carrier having a plurality of rows of solder connections wherein the number of solder connections in at least one row is less than the number of solder connections in each row of solder connections of a subset of the rows of solder connections because of the absence of solder connections at or near one or more corners of the substrate. In addition, claim 29 requires that the substrate is adapted for allowing access through the substrate to one or more solder connections.

In contrast, Lyne only discloses a chip carrier 40 having a footprint of selectively depopulated solder connections 12. The chip carrier 40 in Lyne always has at least one solder connections 12 at each of its four corners. Further, the chip carrier does not have a

through-hole passage or the like at its center. *See* Figs. 6, 9 and 11 of Lyne. Since Moore et al. and Lyne, either alone or jointly, do not teach a substrate having a through-hole channel with an array of solder connections thereon as recited by claim 29, claim 29 is patentable over Moore et al. in view of Lyne.

With respect to the remaining claims, claims 22 and 28 have been discussed above, claims 23 and 25 have been canceled, claim 24 has not been rejected on art, claim 33 is a new claim and both of the are believed patentable in view of the comments set forth above.

In view of the foregoing, the Applicant believes that all of the claims are now in condition for allowance and respectfully requests the Examiner to pass the subject application to issue. If for any reason the Examiner believes any of the claims are not in condition for allowance, he is encouraged to phone the undersigned attorney at (650) 849-7777 so that any remaining issues may be resolved.

Respectfully submitted,

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